## REMARKS

In the Office Action, the Examiner noted that claims 1, 3-23 are pending in the application. The Examiner rejected claims 1 and 3-22, and allowed claim 23. In view of the following discussion, the Applicants submit that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Thus, the Applicants believe that all of these claims are now in condition for allowance.

### I. Rejection of Claims Under 35 U.S.C. §102

**A. Claim 6**

The Examiner rejected claim 6 as being anticipated by Ducaroir (United States patent publication 2001/0043648, published November 22, 2001). The rejection is respectfully traversed.

More specifically, the Examiner stated that Ducaroir discloses a first clock data recovery circuitry for receiving serial data and recovering a first recovered clock from the first serial data ([0020]). The Examiner further stated that Ducaroir discloses a transceiver that provides the first recovered clock and a reference clock and the first serial data to a circuit portion of the transceiver ([0020]). Finally, the Examiner stated that Ducaroir discloses the circuit portion uses one of the first recovered clock and the reference clock for subsequent processing of the first serial data ([0020]). (See Office Action, paragraph 2). The Examiner then concluded that Ducaroir anticipates Applicants' invention as recited in claim 6.

Ducaroir teaches a serial data transceiver to facilitate testing using only the serial data transfer terminals of the transceiver. (See Ducaroir, Abstract). More specifically, Ducaroir teaches that Serializer 18 either uses a reference clock signal to serialize the parallel data during non-test condition, or uses a recovered clock signal to serialize the parallel data during test condition. (See Ducaroir, Paragraph 0021).

Ducaroir, however, does not teach each and every element of Applicants' independent claim 6. Namely, Ducaroir does not teach or suggest using a recovered clock signal and a reference clock signal concurrently to perform processing functions as positively claimed by the Applicants.

In one embodiment, Applicants' invention discloses an approach where the first and second clock based functionalities concurrently perform processing functions using the first recovered clock and the reference clock. (See e.g., Applicants' Specification, paragraphs [0010]-[0011]). In contrast, Ducaroir only discloses using either the reference clock signal or the recovered clock signal for either a test condition or a normal condition, but never concurrently. In other words, Ducaroir specifically teaches away from Applicants' invention where Ducaroir's reference clock signal and the recovered clock signal are only used in a non-concurrent manner. (See Ducaroir, Paragraph [0021]).

Since Ducaroir does not teach the ability to have the first and second clock based functionalities concurrently perform processing functions using the first recovered clock and the reference clock, Ducaroir does not teach each and every element of Applicants' independent claim 6. Accordingly, Ducaroir does not anticipate Applicants' invention recited in claim 6.

**B. Claims 8, 9, 22, and 23**

The Examiner rejected claims 8, 9, 22, and 23 as being anticipated by Ziegler (United States patent publication 2003/0112798, published June 19, 2003). The rejection is respectfully traversed.

More specifically, the Examiner stated that Ziegler discloses a circuitry for receiving a plurality of input serial data streams and that clock data recovery circuitry recovers a corresponding plurality of recovered clocks. Finally, the Examiner stated that Ziegler discloses logic that provides each received input serial data stream to an outgoing transmit block based upon each of the corresponding recovered clocks. (See Office Action, Paragraph 10)

Ziegler teaches a data communication method. Mores specifically, Ziegler teaches a method of communicating a plurality of parallel data packets from a first data parallel bus to a second parallel data bus. (See Ziegler, Abstract).

Ziegler, however, does not teach each and every element of Applicants' independent claim 8. Namely, Ziegler does not teach or suggest using a plurality of

recovered clock signals from a plurality of serial data and a reference signal as positively claimed by the Applicants.

In one embodiment, Applicants' invention discloses an approach where a plurality of recovered clocks and a reference clock are provided to a circuit portion where one of the clocks is used for processing one of the serial data. (See e.g., Applicants' Specification, paragraphs [0010]-[0011]). In contrast, Ziegler only discloses an approach for providing a plurality of recovered clock signals but does not provide a reference clock for processing one of the serial data.

The Examiner in Paragraph 2 of the Office Action argued that Applicants' claim 8 "does not contain the limitation 'using a plurality of recovered clock signals'". Applicants respectfully disagree. Applicants' claim 8 recites "clock data recovery circuitry for recovering a corresponding plurality of recovered clocks based on the plurality of input serial data streams" and that "wherein the logic provides each received input serial data stream of the plurality of input serial data streams to the outgoing transmit block based upon each corresponding recovered clock of the plurality of corresponding recovered clocks or said reference clock". In other words, since the logic provides each received input serial data stream to the outgoing transmit block based upon each corresponding recovered clock, it is absolutely clear that Applicants' invention is using a plurality of recovered clock signals.

Since Ziegler does not teach an approach where a plurality of recovered clocks and a reference clock are provided to a circuit portion where one of the clocks is used for processing one of the serial data, Ziegler does not teach each and every element of Applicants' independent claim 8. Accordingly, Ziegler does not anticipate Applicants' invention as recited in claim 8.

Similarly, since Ziegler does not teach an approach where a plurality of recovered clocks and a reference clock are provided to a circuit portion where one of the clocks is used for processing one of the serial data, Ziegler does not teach each and every element of Applicants' independent claim 22. Namely, claim 22 recites a method of clock management that uses a plurality of recovered clock signals from a plurality of data streams and a reference clock signal. Accordingly, Ziegler does not anticipate Applicants' invention as recited in claim 22.

Finally, claim 9 depends from claim 8 and recites additional features therefor. Since Ziegler does not anticipate Applicants' invention as recited in claim 8, dependent claim 9 is also not anticipated and is allowable. Therefore, the Applicants contend that claims 8, 9, and 22 are not anticipated by Ziegler and, as such, fully satisfy the requirements of 35 U.S.C. §102.

It should be noted that although the Examiner indicated in Paragraph 10 that claim 23 is rejected, the Examiner also indicated that claim 23 is allowed in Paragraphs 2 and 18 of the Office Action and in the Office Action Summary. As such, responsive to the Examiner, Applicants will presume that claim 23 is currently allowed.

II. Rejection Of Claims Under 35 U.S.C. §103

**A. Claims 1 and 4**

The Examiner rejected claims 1 and 4 as being unpatentable over Ducaroir in view of Ziegler. The rejection is respectfully traversed.

More specifically, the Examiner conceded that Ducaroir does not teach a delay locked loop circuitry for receiving a second serial data to produce a second received clock. The Examiner stated, however, that Ziegler teaches a second clock recovery circuit. (See Office Action, paragraph 12). The Examiner concluded that it would have been obvious to combine the second clock recovery circuitry of Ziegler with the teaching of Ducaroir. Applicants respectfully disagree.

As discussed above, Ducaroir only discloses the use of a single recovered clock with a reference clock, whereas Ziegler only discloses the use of multiple recovered clocks but does not use a reference clock for processing one of a plurality of serial data. Thus, it is respectfully submitted that Ducaroir teaches away from Ziegler. For example, Ziegler does disclose a reference clock, but it is not used for processing one of a plurality of serial data. As such, the Examiner cannot combine Ducaroir with Ziegler to make Applicants' independent claims 1 and 4 obvious.

The Examiner also argued in Paragraph 1 of the Office Action that Applicants' claim 1 does not contain any limitation directed toward recovering a plurality of recovered clock signals from a plurality of serial data. Applicants respectfully disagree. Specifically, Applicants' claim 1 recites "first clock data recovery circuitry for

receiving first serial data and recovering a first recovered clock from the first serial data" and "a second clock data recovery circuitry for receiving second serial data and recovering a second recovered clock from the second serial data". Since two recovered clocks are recovered from two serial data, then it is absolutely clear that Applicants' claim 1 recites recovering a plurality of recovered clock signals from a plurality of serial data.

Therefore, Applicants contend that claims 1 and 4 are patentable over the combination of Ducaroir and Ziegler and, as such, fully satisfy the requirements of 35 U.S.C. §103.

**B. Claim 3**

The Examiner rejected claim 3 as being unpatentable over Ducaroir in view of Ziegler and further in view of Talbot (US Publication No. 20040014448). The rejection is respectfully traversed.

More specifically, the Examiner conceded that Ducaroir does not teach a delay locked loop circuitry for receiving a second serial data to produce a second received clock. The Examiner stated, however, that Ziegler teaches a second clock recovery circuit. The Examiner then conceded that Ziegler is still deficient because Ziegler fails to disclose a delay locked loop circuitry for receiving second serial data to produce a second recovered clock from the second serial data. (See Office Action, paragraph 13). However, the Examiner alleged that Talbot teaches a clock recovery delay locked loop. The Examiner concluded that it would have been obvious to combine the second clock recovery circuitry of Ziegler and the clock recovery delay locked loop of Talbot with the teaching of Ducaroir. Applicants respectfully disagree.

As discussed above, Ducaroir only discloses the use of a single recovered clock with a reference clock, whereas Ziegler only discloses the use of multiple recovered clocks but does not use a reference clock for processing one of a plurality of serial data. Similarly, Talbot also fails to disclose the use of a reference clock for processing one of a plurality of serial data. Thus, it is respectfully submitted that Ducaroir teaches away from Ziegler and Talbot. For example, Ziegler does disclose a reference clock, but it is not used for processing one of a plurality of serial data.

Similarly, Talbot does not even disclose the use of a reference clock at all. As such, the Examiner cannot combine Ducaroir with Ziegler and Talbot to make Applicants' independent claim 1 obvious.

The Examiner in Paragraph 3 of the Office Action argued that Applicants cannot attack the cited references individually in a 103 rejection. Applicants respectfully submit that Applicants are not attacking the references individually. Contrary to the Examiner's position, Applicants are addressing the combination of all three (3) references. More specifically, Applicants are directing the Examiner's attention to the fact that one of ordinary skill in the art would not combine these three references to make Applicants' invention obvious. Applicants' position is clearly supported by the fact that the teachings of these references would actually teach away from their combination. The Examiner must evaluate the teaching of each reference as a whole and cannot simply select bits and pieces out of each of the references and then broadly state that their combination would make Applicants' obvious. The Examiner must present a prima facie case supporting the obviousness rejection as to why one of ordinary skill in the art would combine these references to arrive at Applicants' invention. It is respectfully submitted that the Examiner has failed to present a prima facie case of obviousness in the present instance.

Claim 3 depends from claim 1 and recites additional features therefor. Thus, the cited references, either singly or in any permissible combination, also do not teach, suggest, or otherwise render obvious Applicants' invention recited in claim 3. Therefore, Applicants contend that claim 3, which depends from claim 1, is patentable over the combination of Ducaroir, Ziegler and Talbot and, as such, fully satisfies the requirements of 35 U.S.C. §103.

**C. Claim 5**

The Examiner rejected claim 5 as being unpatentable over Ducaroir in view of Ziegler and further in view of Jordan (United States patent publication 2004/0133734, published July 8, 2004). The rejection is respectfully traversed.

More specifically, the Examiner conceded that Ducaroir and Ziegler do not teach a programmable logic fabric. The Examiner stated, however, that Jordan

teaches a programmable logic fabric for providing the advantage of flexibility in the configuration of functional models. (See Office Action, Paragraph 14). The Examiner concluded that it would have been obvious to combine the programmable logic fabric of Jordan with the teaching of Ducaroir and Ziegler. Applicants respectfully disagree.

It is respectfully submitted that Ducaroir, Ziegler and Jordan are not in analogous arts. Specifically, Ducaroir discloses a serial data transceiver and Ziegler discloses a data communication method, whereas Jordan discloses a method to hide an operating system program in a memory block. Therefore, any combination of Ducaroir, Ziegler and Jordan would be impermissible use of hindsight.

Claim 5 depends from claim 1 and recites additional features therefor. Thus, the cited references, either singly or in any permissible combination, also do not teach, suggest, or otherwise render obvious Applicants' invention recited in claim 5. Therefore, Applicants contend that claim 5, which depends from claim 1 is patentable over the combination of Ducaroir, Ziegler and Jordan and, as such, fully satisfies the requirements of 35 U.S.C. §103.

**D. Claims 10, 11, 12, and 14-16**

The Examiner rejected claims 10, 11, 12, and 14-16 as being unpatentable over Ducaroir in view of Jordan. The rejection is respectfully traversed.

As discussed above, it is respectfully submitted that Ducaroir and Jordan are not in analogous arts. Specifically, Ducaroir discloses a serial data transceiver, whereas Jordan discloses a method to hide an operating system program in a memory block. Therefore, any combination of Ducaroir and Jordan would be impermissible use of hindsight. Therefore, Applicants contend that independent claims 10 and 14 are patentable over the combination of Ducaroir and Jordan and, as such, fully satisfy the requirements of 35 U.S.C. §103.

Claims 11, 12, and 15-16 depend from claims 10 and 14 and recite additional features therefor. Thus, the cited references, either singly or in any permissible combination, also do not teach, suggest, or otherwise render obvious Applicants' invention recited in claims 11, 12, and 15-16. Therefore, Applicants contend that claims 11, 12, and 15-16, which depends from claims 10 and 14, are patentable over

the combination of Ducaroir and Jordan and, as such, fully satisfy the requirements of 35 U.S.C. §103.

**E. Claims 13, 17 and 18**

The Examiner rejected claims 13, 17 and 18 as being unpatentable over Ducaroir in view of Jordan and further in view of Ziegler. The rejection is respectfully traversed.

More specifically, the Examiner conceded that Ducaroir and Jordan do not teach a second clock recovery. The Examiner stated, however, that Ziegler teaches recovering a second recovered clock. (See Office Action, Paragraph 16). The Examiner concluded that it would have been obvious to combine the recovering of a second recovered clock of Ziegler with the teaching of Ducaroir and Jordan. Applicants respectfully disagree.

It is respectfully submitted that Ducaroir, Ziegler and Jordan are not in analogous arts. Specifically, Ducaroir discloses a serial data transceiver and Ziegler discloses a data communication method, whereas Jordan discloses a method to hide an operating system program in a memory block. Therefore, any combination of Ducaroir, Ziegler and Jordan would be impermissible use of hindsight.

Claims 13, 17 and 18 depend from claims 10 and 14, respectively and recite additional features therefor. Thus, the cited references, either singly or in any permissible combination, also do not teach, suggest, or otherwise render obvious Applicants' invention recited in claims 13, 17 and 18. Therefore, Applicants contend that claims 13, 17 and 18, which depend from claims 10 and 14 are patentable over the combination of Ducaroir, Ziegler and Jordan and, as such, fully satisfy the requirements of 35 U.S.C. §103.

**F. Claims 19-21**

The Examiner rejected claims 19-21 as being unpatentable over Ziegler in view of Knapp (United States patent publication 2005/0053179, published on February 3, 2005). The rejection is respectfully traversed.

The Examiner conceded that Ziegler fails to disclose a circuit portion that chooses among the first and second recovered clocks and a reference clock for subsequent processing. However, the Examiner alleged that Knapp chooses a recovered clock and a reference clock for subsequent processing.

The Examiner's attention is directed to the fact that neither Ziegler nor Knapp discloses or teaches choosing among the first and second recovered clocks and a reference clock for subsequent processing. More specifically, Knapp only discloses choosing between a single recovered clock and a reference signal. As such, Knapp does not bridge the significant gap left by Ziegler. In other words, even if Ziegler and Knapp were to be allowed to be combined, they would still fail to teach or suggest all the elements of Applicants' independent claim 19. As such, independent claim 19 is patentable over the combination of Ziegler and Knapp.

Claims 20-21 depend from claim 19 and recite additional features therefor. Thus, the cited references, either singly or in any permissible combination, also do not teach, suggest, or otherwise render obvious Applicants' invention recited in claims 20-21. Therefore, Applicants contend that claims 20-21, which depend from claim 19, are patentable over the combination of Ziegler and Knapp and, as such, fully satisfy the requirements of 35 U.S.C. §103.

III. Allowed claim

The Applicants express their appreciation for the indication that claim 23 is allowed.

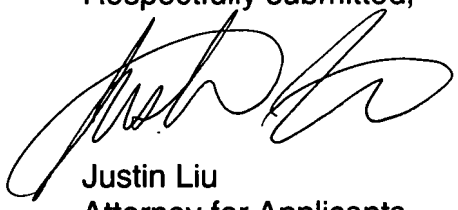
## CONCLUSION

Thus, the Applicants submit that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Consequently, the Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Justin Liu at 408-879-4641 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,



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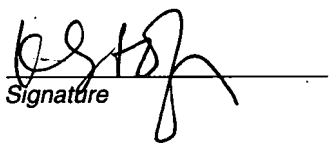

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